

JPE 8-3-7

A Three-Phase Four-Wire DSTATCOM for Power Quality Improvement

Bhim Singh*, P. Jayaprakash[†] and D. P. Kothari**

[†]Dept. of Electrical Engineering, Indian Institute of Technology, Delhi, India

^{**}Vellore Institute of Technology, India

ABSTRACT

Power quality improvement in a three-phase four-wire system is achieved using a new topology of DSTATCOM (distribution static compensator) consisting of a star/delta transformer with a tertiary winding and a three-leg VSC (voltage source converter). This new topology of DSTATCOM is proposed for power factor correction or voltage regulation along with harmonic elimination, load balancing and neutral current compensation. A tertiary winding is introduced in each phase for a delta connected secondary in addition to the star-star windings and this delta connected winding is responsible for neutral current compensation. The dynamic performance of the proposed DSTATCOM system is demonstrated using MATLAB with its Simulink and Power System Blockset (PSB) toolboxes under varying loads. The capacitor supported DC bus of the DSTATCOM is regulated to the reference voltage under varying loads.

Keywords: Power Quality Improvement, DSTATCOM, 3-leg VSC, Star-delta transformer, Neutral current compensation

1. Introduction

The AC distribution systems are facing severe power quality problems due to the proliferation of non-linear loads and single-phase loads. Some of these power quality problems include high reactive power burden, harmonic currents, load unbalance, excessive neutral current, etc. [1-5]. The power quality at the PCC (point of common coupling) is governed by standards such as IEEE-519; IEC 1000 standards are also widely accepted [6-7]. The group of controllers used in the distribution system for power

quality improvement in three-phase four-wire systems is known as custom power devices (CPD) [2]. These custom power devices include the DSTATCOM (distribution static compensator), DVR (dynamic voltage restorer) and UPQC (unified power quality conditioner). The DSTATCOM is a shunt-connected device, which takes care of the power quality problems in the currents.

Three-phase four-wire active compensators are used for neutral current compensation along with reactive power compensation for voltage regulation or power factor correction, harmonic elimination and load balancing in a three-phase four-wire system with linear and non-linear loads [8-10]. There are four different topologies reported in the literature for a three-phase four-wire DSTATCOM, such as a four-leg VSC (Voltage Source Converter) based, three-leg VSC with split capacitors, three single-phase

Manuscript received April 17, 2008; revised May 28, 2008

[†]Corresponding Author : jayaprakashpee@gmail.com

Tel: +91-011-2659-1045, Fax: +91-011-2658-1606, IIT, India

*Dept. of Electrical Engineering, IIT, Delhi, India

**Vellore Institute of Technology, India

VSC based ^[4] and three-leg VSC with a zig-zag transformer ^[10]. There are many control schemes reported in the literature for control of shunt active compensators like instantaneous reactive power theory, power balance theory, synchronous reference frame theory, symmetrical components based, etc. ^[9]. The application of a zig-zag transformer for reduction of a neutral current is advantageous due to passive compensation and ruggedness ^[10]. In a similar way, a star-delta transformer is also used for neutral current compensation in a three-phase four-wire distribution system ^[11-14]. Moreover, in a three-phase three-wire system, a star/delta transformer is used for isolation of the three-leg VSC based DSTATCOM ^[15]. The voltage regulation at the PCC can be achieved using a shunt compensator and the stability is improved when it also performs harmonic elimination ^[16].

In this paper, a new topology is proposed for the DSTATCOM in which a three-leg VSC is integrated with a star-delta transformer to perform the compensations required for a three-phase four-wire system. In order to optimize the voltage rating of the three-leg VSC and to provide isolation to the VSC, it is connected across a tertiary winding in each phase of the transformer secondary. The dynamic performance is studied for voltage regulation and power factor correction modes of the DSTATCOM. The DSTATCOM features the following characteristics.

- a) Use of readily available three -phase three-leg VSC
- b) Neutral current compensation during linear and non linear loads using a star-delta transformer
- c) Isolated operation of the three-leg VSC as it is integrated with the star-delta transformer
- d) Harmonic current compensation and load balancing
- e) Reactive current compensation for unity power factor (UPF) or the zero voltage regulation (ZVR) at the point of common coupling (PCC)
- f) Capacitor supported operation of DSTATCOM

2. Principle Of Operation of DSTATCOM

Fig. 1(a) shows the single line diagram of a DSTATCOM system. The inductor (L_s) and the resistor (R_s) correspond to the line inductance and the effective resistance of the line respectively. The capacitor, C_f and

resistor, R_f in Fig.2 represent the ripple filter installed for filtering the high frequency switching noise of the voltage at PCC. Fig. 1(b) shows the phasor diagram of the system for unity power factor (UPF) operation. The reactive current (I_c) injected by the DSTATCOM is to cancel the reactive power component of the load current so that the source current is reduced to an active power component of the load current only (I_s). These currents are adjusted dynamically to maintain unity power factor under varying load conditions. Fig. 1(c) shows the phasor diagram for a zero voltage regulation (ZVR) operation. In this mode, DSTATCOM injects a current I_c , such that the voltage at PCC (V_s) and source voltage (V_M) are in the locus of the same circle.

The three-phase four-wire DSTATCOM is used for reactive power compensation, harmonics currents elimination, load balancing and neutral current compensation. Fig. 2 shows the power circuit of the proposed DSTATCOM consisting of a three-leg VSC integrated with a star/delta transformer. The star connected primary windings are connected to the supply at the PCC and the delta connected secondary winding provides a circulating path for the zero sequence current. A set of third windings is designed in the secondary transformer for connecting the three-leg VSC. This transformer provides isolation to the DSTATCOM as well as the suitability of selecting an 'off the shelf' three-phase VSC for this application. The DSTATCOM provides neutral current compensation, harmonic elimination and load balancing along with power factor correction or line voltage regulation. The detailed design of the DSTATCOM, the star/delta transformer and control of the system are given in the following sections.

2.1 Design of Three-Phase DSTATCOM

A three-leg, PWM controlled IGBT based voltage source converter (VSC) is used as a DSTATCOM. The rating of the IGBT (insulated gate bipolar transistor) switches is based on the voltage and current rating of the compensation system. For the considered load mentioned in the Appendix, the rating of the VSC for reactive power compensation is found to be 12 kVA. The selection of the DC bus voltage, a DC bus capacitor, an AC inductor and the ripple filter are given below as ^[17]:

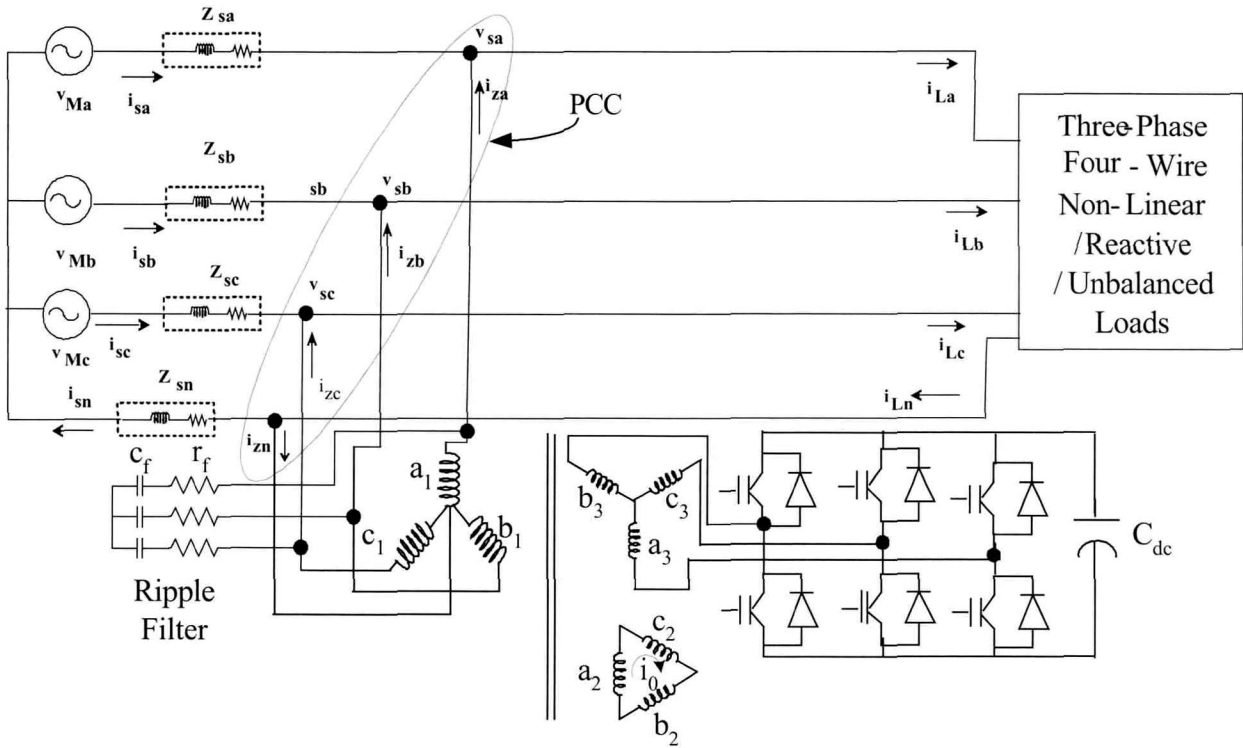


Fig. 2 Schematics of proposed Integrated 3-leg VSC with star/star-delta transformer based DSTATCOM connected in distribution system

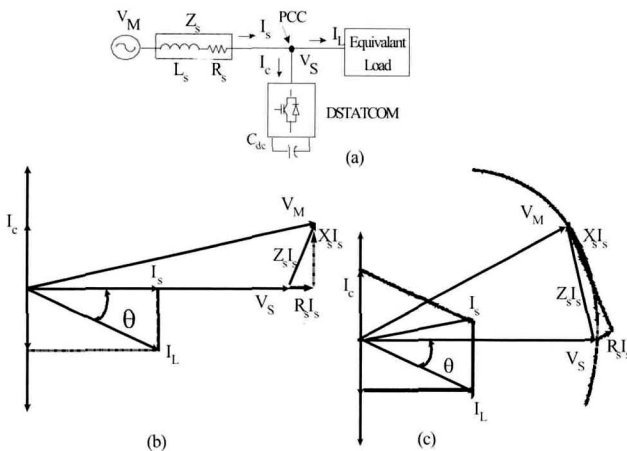


Fig. 1 (a) Single line diagram of a DSTATCOM
(b) Phasor diagram for UPF operation
(c) ZVR operation

(i) DC Bus Voltage:

The value of a DC bus voltage (V_{dc}) depends on the instantaneous energy available to the DSTATCOM. For a three-phase VSC, the DC bus voltage is defined as

$$V_{dc} = 2\sqrt{2}V_{LL} / (\sqrt{3}m) \tag{1}$$

where m is the modulation index and is considered as 1 and V_{LL} is the AC line output voltage of DSTATCOM. Thus V_{dc} is obtained as 326.54V for V_{LL} of 200V and is selected as 400V.

(ii) DC Bus Capacitor:

The design of the DC capacitor is governed by the reduction in the DC bus voltage upon application of the load and rise in the DC bus voltage for the removal of the load. Using the principle of energy conservation, the equation governing C_{dc} is as,

$$\frac{1}{2}C_{dc}[(V_{dc}^2) - (V_{dc1}^2)] = 3V(aI)t \tag{2}$$

where V_{dc} is the reference DC voltage and V_{dc1} is the minimum voltage level of the DC bus, a is the over loading factor, V is the phase voltage, I is the phase current of the

VSC and t is time for which the DC bus voltage is to be recovered.

Considering, $V_{dc} = 400V$, $V_{dc1} = 390V$, $V = 239.60V$, $I = 27.82A$, $t = 350 \mu s$, $a = 1.2$, the calculated value of C_{dc} is $2176 \mu F$ and $\#$ is selected as $2200 \mu F$.

(iii) *AC inductor:*

The selection of the AC inductance (L_f) depends on the current ripple, $i_{cr,p-p}$, switching frequency f_s , DC bus voltage (V_{dc}) and the L_f is given as ^[17]

$$L_f = \left(\sqrt{3} m V_{dc} \right) / (12 a f_s i_{cr(p-p)}) \quad (3)$$

where m is the modulation index and a is the over load factor. Considering, $i_{cr,p-p} = 5\%$, $f_s = 10 \text{ kHz}$, $m = 1$, $V_{dc} = 400V$, $a = 1.2$, the L_f value is calculated to be 3.44 mH . The round off value of L_f of 3.5 mH is selected in this investigation.

(iv) *Ripple Filter:*

A low-pass first order filter tuned at half the switching frequency is used to filter the high frequency noise from the voltage at the PCC. Considering a low impedance of 3Ω for the harmonic voltage at a frequency of 5 kHz , the ripple filter capacitor is designed as $C_f = 5 \mu F$. A series resistance (R_f) of 5Ω is included in series with the capacitor (C_f). The impedance is found to be 637Ω at fundamental frequency, which is sufficiently large.

2.2 Design of Star /Star-Delta Transformer

The delta connected secondary winding of the transformer provides a path for the zero sequence fundamental current and harmonic currents and hence, offers a path for the neutral current when connected in shunt at PCC ^[11-12]. Under a single-phase load, the zero sequence load neutral current circulates in the delta windings of the star-delta transformer. The voltage across each primary winding is the phase voltage. In order to connect the DSTATCOM to this transformer, a set of third windings in each phase is introduced at its secondary as shown in Fig. 3. The voltage rating of the star-delta transformer windings are shown in the Appendix.

2.3 Control of DSTATCOM

There are many control approaches available for the generation of reference source currents for the control of VSC of DSTATCOM for a three-phase, four-wire system in literature ^[9-10]. The synchronous reference frame theory is used for the control of a three-phase three-leg VSC of the DSTATCOM. A block diagram of the control scheme is shown in Fig. 4. The load currents (i_{La} , i_{Lb} , i_{Lc}), the PCC voltages (v_{Sa} , v_{Sb} , v_{Sc}) and DC bus voltage (v_{dc}) of DSTATCOM are sensed as feedback signals. The load currents in the three phases are converted into the d-q-0 frame using the Park's transformation as in eqn. (4).

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \theta & -\sin \theta & \frac{1}{2} \\ \cos \left(\theta - \frac{2\pi}{3} \right) & -\sin \left(\theta - \frac{2\pi}{3} \right) & \frac{1}{2} \\ \cos \left(\theta + \frac{2\pi}{3} \right) & \sin \left(\theta + \frac{2\pi}{3} \right) & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (4)$$

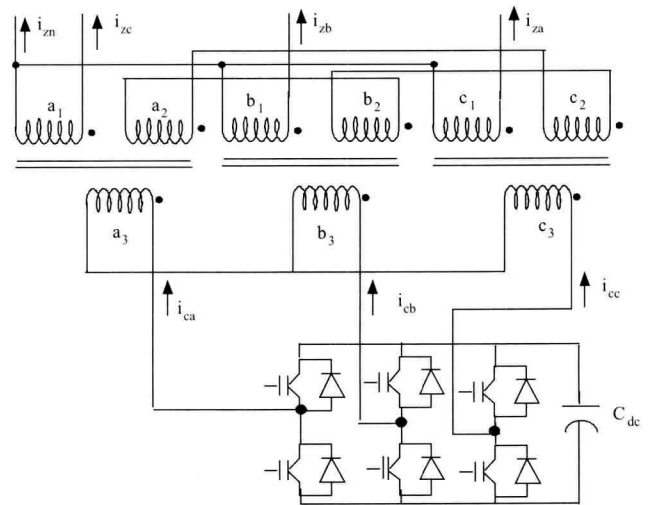


Fig. 3 Star/star-delta transformer and the three-leg VSC for operation as DSTATCOM

A three-phase PLL (phase locked loop) is used to synchronize these signals with the PCC voltage. The d-q components are then passed through low pass filters to extract the DC components of i_d and i_q . The error between the reference DC capacitor voltage and the sensed DC bus voltage of DSTATCOM is given to a PI (proportional-integral) controller and its output voltage is considered as the loss component of the current and is

added to the DC component of i_d . Similarly, a second PI controller is used to regulate the PCC voltage. The amplitude of PCC voltage and its reference value are fed to a PI controller and the output of the PI controller is added with the DC component of i_q . The control strategy is to regulate the PCC voltage, elimination of harmonics in load currents and the load balancing. The resultant d-q currents are again converted into the reference source currents using the reverse Park's transformation. Here the three phase source currents are controlled using a PWM current controller to generate gating pulses for the IGBT switches. For power factor correction operation of DSTATCOM, only the DC bus voltage PI controller is required in the control algorithm.

3. Modeling and Control of DSTATCOM

The three-leg VSC and the star/star-delta transformer based DSTATCOM connected to a three-phase four-wire system is modeled and simulated using the MATLAB and its Simulink and Power System Blockset toolboxes. The DSTATCOM system shown in Fig. 2 is modeled in MATLAB. The ripple filter is connected to the DSTATCOM for filtering the ripple in the PCC voltage. The system data is given in the Appendix.

The control algorithm for the DSTATCOM is also modeled in MATLAB. The reference source currents are

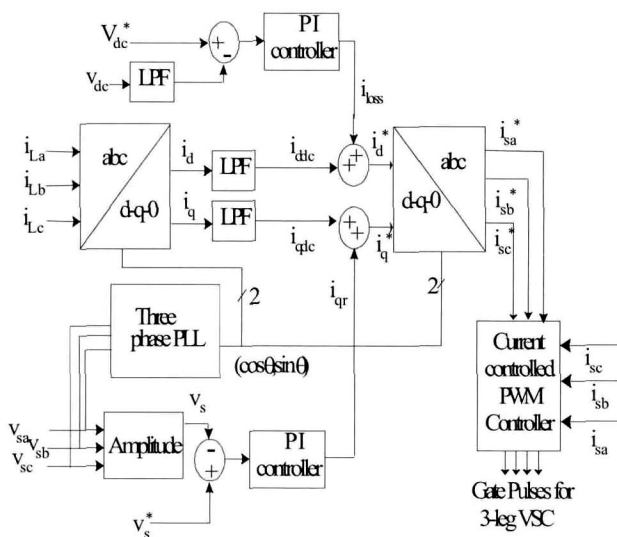


Fig. 4 Control algorithm for the three-leg VSC based DSTATCOM in a three phase 4-wire system

derived from the sensed PCC voltages (v_{sa}, v_{sb}, v_{sc}), load currents (i_{La}, i_{Lb}, i_{Lc}) and the DC bus voltage of DSTATCOM (v_{dc}). A pulse width modulated (PWM) current controller is used over the reference and sensed source currents to generate the gating signals for the IGBTs of the VSC of the DSTATCOM.

4. Results and Discussion

The performance of a three-leg VSC and the star/star-delta transformer based DSTATCOM for PCC voltage regulation, along with neutral current compensation and load balancing of a three-phase four-wire load is shown in Fig. 5. The PCC voltages (v_s), balanced source currents (i_s), load currents (i_L), compensator currents (i_c), load neutral current (i_{Ln}), compensator neutral current (i_{cn}), source neutral current (i_{sn}), DC bus voltage (v_{dc}) and the amplitude of PCC voltage (V_s) are demonstrated under a change of load conditions. It is observed that the amplitude of PCC voltage is regulated to the reference amplitude by injecting the required reactive power compensation. The zero sequence fundamental current of the load neutral current resulted from the unbalanced load currents is circulated in the star-delta transformer and hence, the source neutral current is maintained at nearly zero. The DC voltage of VSC is maintained near the reference DC voltage under all load disturbances. Fig. 6 shows the dynamic performance of the proposed DSTATCOM system for harmonic elimination along with voltage regulation, load balancing and neutral current compensation. The PCC voltages (v_s), balanced source currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_c), load neutral current (i_{Ln}), compensator neutral current (i_{cn}), source neutral current (i_{sn}), DC bus voltage (v_{dc}) and amplitude of PCC voltage (V_s) are shown under varying non-linear loads. The zero sequence harmonic and fundamental neutral currents are circulated in the star-delta transformer and hence, the supply neutral current is nearly zero.

The dynamic performance of DSTATCOM with the star-delta transformer for neutral current compensation along with load balancing in the unity power factor (UPF) mode of operation is depicted in Fig. 7. The PCC voltages (v_s), balanced source currents (i_s), load currents (i_L),

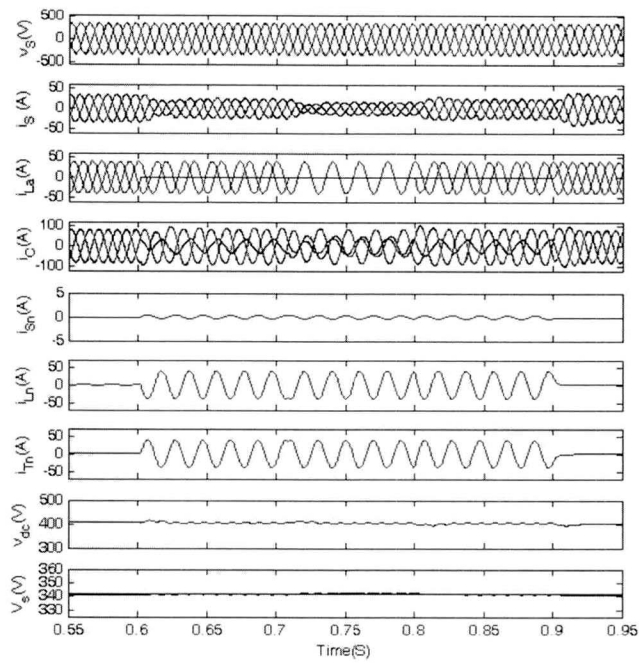


Fig. 5 Performance of 3-phase Three-leg VSC and star/star-delta transformer based DSTATCOM for neutral current compensation, load balancing and voltage regulation

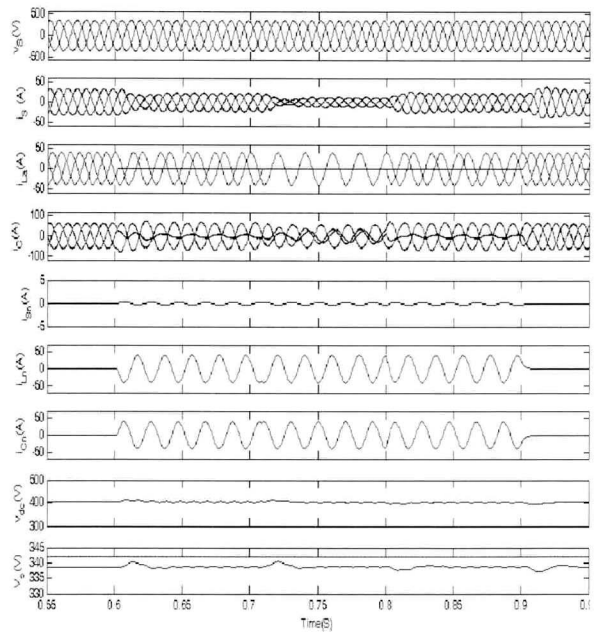


Fig. 7 Performance of 3-phase Three-leg VSC and star/star-delta transformer based DSTATCOM for neutral current compensation, load balancing and power factor correction

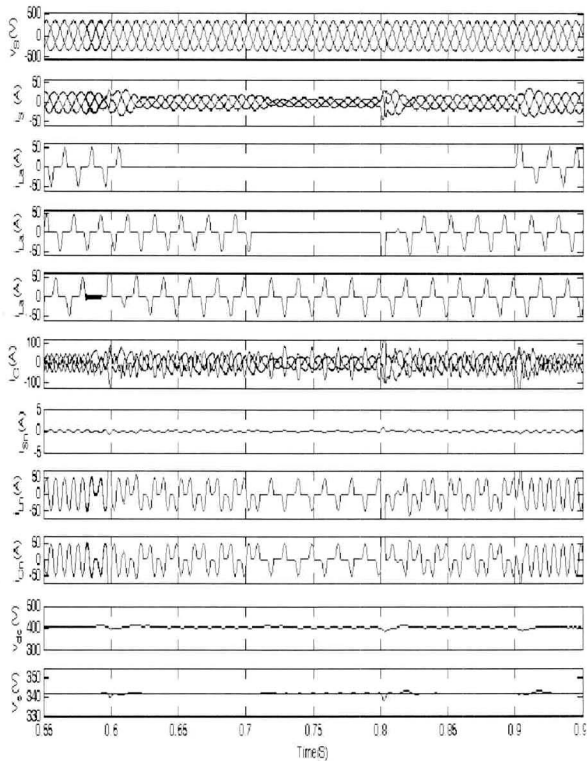


Fig. 6 Performance of 3-phase Three-leg VSC and star/star-delta transformer based DSTATCOM for neutral current compensation, load balancing, harmonic compensation and voltage regulation

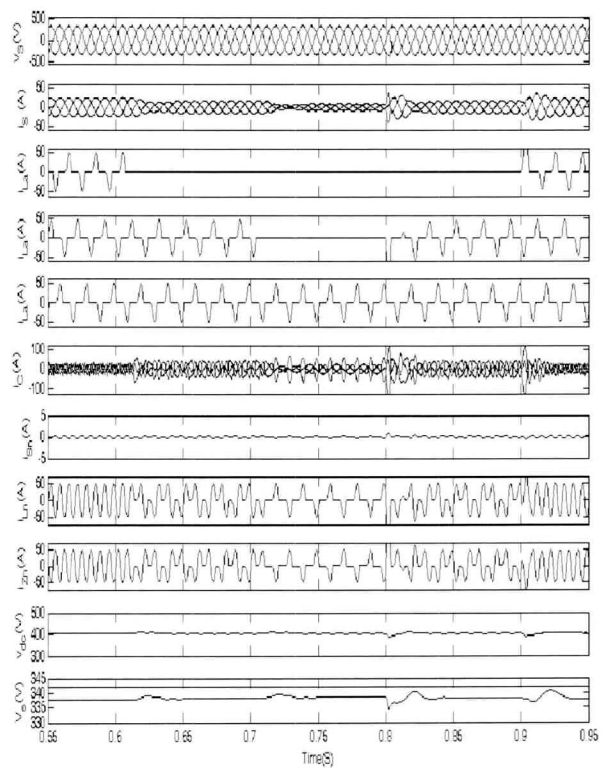


Fig. 8 Performance of 3-phase Three-leg VSC and star/ star-delta transformer based DSTATCOM for neutral current compensation, load balancing, harmonic compensation and power factor correction

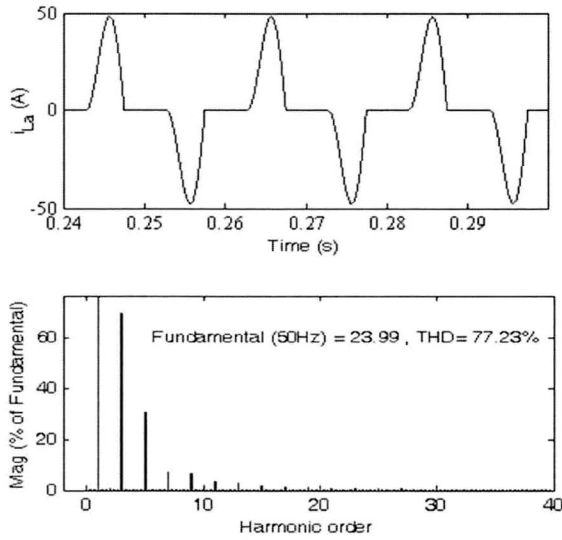


Fig. 9 Load current and the harmonic spectrum

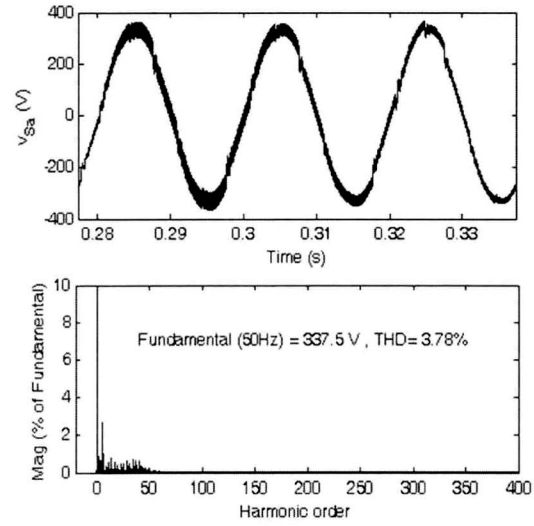


Fig. 11 Voltage at PCC without compensator

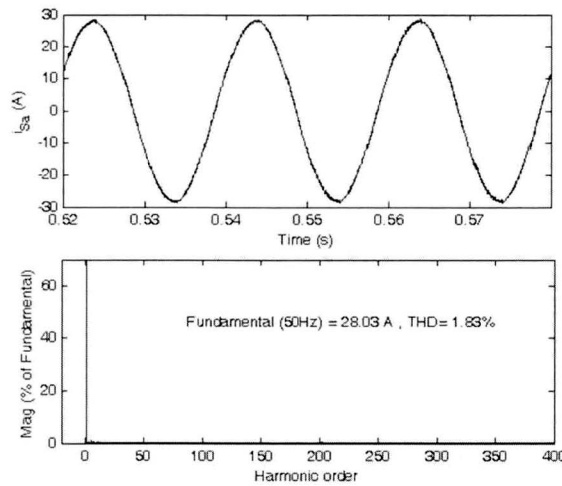


Fig. 10 Source current and the harmonic spectrum

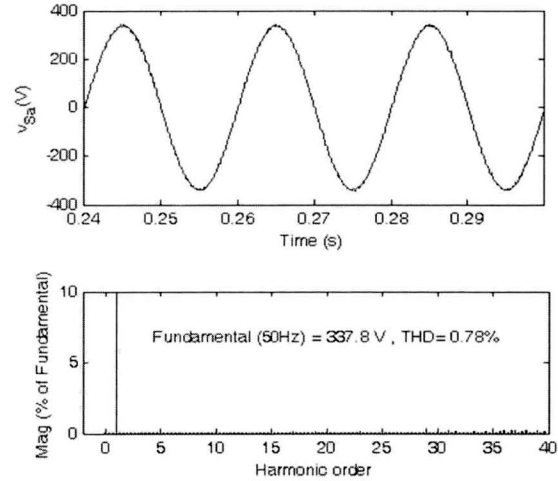


Fig. 12 Voltage at PCC with compensator

compensator currents (i_c), load neutral current (i_{Ln}), compensator neutral current (i_{cn}), source neutral current (i_{sn}), DC bus voltage (v_{dc}) and amplitude of PCC voltage (V_s) are demonstrated under varying loads. It is also observed that the PCC voltage is not regulated in this case as the compensator is operated in the UPF mode. Fig. 8 shows the dynamic performance of DSTATCOM with the star-delta transformer for harmonic elimination along with neutral current compensation and load balancing in the unity power factor (UPF) mode of operation. The waveform of load current and its harmonic spectrum is shown in Fig. 9 and the compensated source current with

its harmonic spectrum is shown in Fig. 10. The voltage at the PCC with its harmonic spectrum when the DSTATCOM is not in operation is shown in Fig.11 and with DSTATCOM in operation is shown in Fig. 12. It may be observed that the THD (total harmonic distortion) of the source current is reduced less than 5% thus meeting the requirement of IEEE-519 standard [7].

5. Conclusions

The modeling and simulation of a new topology of DSTATCOM consisting of three-leg VSC integrated with

a star/star-delta transformer with a tertiary winding has been carried out and the performance has been demonstrated for neutral current compensation along with reactive power compensation, harmonic elimination and load balancing. The voltage regulation and power factor correction modes of operation of the DSTATCOM have been observed as expected ones. The star/delta transformer has been found effective for compensating the zero sequence fundamental and harmonics currents. The DC bus voltage of the DSTATCOM has been regulated to the reference DC bus voltage under all varying loads.

Appendix

Line Impedance: $R_s=0.01 \Omega$, $L_s= 2 \text{ mH}$

Loads: (i) Linear: 20 kVA, 0.80 pf lag

(ii) Non-linear: Three single-phase bridge rectifier with $R = 25 \Omega$ and $C = 470\mu\text{F}$

Ripple filter: $R_f= 5 \Omega$, $C_f= 5 \mu\text{F}$

DSTATCOM:

DC bus capacitance of DSTATCOM: 2200 μF

DC bus voltage of DSTATCOM: 400 V

DC voltage PI controller: $K_p=0.1$, $K_i=0.8$

PCC voltage PI controller: $K_p=0.2$, $K_i=0.5$

AC line voltage: 415 V, 50 Hz

PWM switching frequency: 10 kHz

Star-Delta Transformer:

Three numbers of single-phase transformers of each of rating 5kVA, 250V/150V/150V.

References

- [1] E.Acha, V.G. Agelids, O. Anaya-Lara, T.J.E. Miller, *Power Electronic Control in Electric Systems*, Newness Power engineering series, 1st Edition, Oxford, 2002.
- [2] A.Ghosh and G. Ledwich, *Power Quality Enhancement using Custom Power devices*, Kluwer Academic Publishers, London, 2002.
- [3] R. C. Dugan, M. F. McGranaghan and H. W. Beaty, *Electric Power Systems Quality*. 2nd Edition, McGraw Hill, New York, 2006.
- [4] H. Akagi, E. H. Watanabe and M. Aredes, *Instantaneous power theory and applications to power conditioning*, John Wiley & Sons, New Jersey, USA, 2007.
- [5] Antonio Moreno-Munoz, *Power Quality: Mitigation Technologies in a Distributed Environment*, Springer-Verlag London limited, London, 2007.
- [6] *IEEE Recommended Practices and Requirements for Harmonics Control in Electric Power Systems*, IEEE Std. 519, 1992.
- [7] *Electromagnetic Compatibility (EMC) – Part 3: Limits-Section 2: Limits for harmonic current emissions (equipment input current <16 A per phase)*, IEC1000-3-2 Document, First Edition, 1995.
- [8] M.C. Benhabib and S. Saadate, "New control approach for four-wire active power filter based on the use of synchronous reference frame", *Electric Power Systems Research*, Vol. 73, No. 3, pp. 353-362, Mar. 2005.
- [9] María Isabel Milanés, Enrique Romero Cadaval and Fermín Barrero González, "Comparison of Control Strategies for Shunt Active Power Filters in Three-Phase Four-Wire Systems", *IEEE Transactions on Power Electronics*, Vol. 22, No. 1, pp.229-236, Jan. 2007.
- [10] Hurng-Liahng, Kuen- Der Wu, Jinn- Chang Wu and Wen-Jung Chiang, "A three-phase four- wire power filter comprising a three-phase three-wire active filter and a zig-zag transformer", *IEEE Trans. of Power Electronics.*, Vol. 23, No. 1, pp. 252-259, Jan. 2008.
- [11] Sikyung Kim, Prasad N. Enjeti and Ira J. Pitel, "A New approach to improve power factor and reduce harmonics in a three-phase diode rectifier type utility interface", *IEEE Trans. Ind. Applicat.*, Vol. 30, No. 6, pp. 1557-1564, Nov./ Dec. 1994.
- [12] P. Enjeti, W. Shireen, P. Packebush and I. Pitel, "Analysis and Design of a New Active Power Filter to Cancel Neutral Current Harmonics in Three-phase Four-Wire Electric Distribution Systems", *IEEE Trans. Ind. Applicat.*, Vol. 30, No. 6, pp. 1565-1572, Nov./ Dec. 1994.
- [13] Steffan Hansen, Peter Nielsen and Frede Blaabjerg, "Harmonic Cancellation by mixing Non-linear single-phase and three-phase loads", *IEEE Trans. Ind. Applicat.*, Vol.36, No.1, pp.152-159, Jan./Feb. 2000.
- [14] P. Vedelho and G. D. Marques, "A neutral current electronic compensator", *Proc. of IEEE Proceedings in Industrial Electronics*, Vol.2, pp. 831-836, Aug/Sept 1998.
- [15] M.G.Molina and P.E.Mercado, "Control Design and Simulation of DSTATCOM with Energy Storage for Power Quality Improvements", in *Proc. of TDC 06*, pp. 1-7, Aug. 2006.
- [16] H. Fugita and H. Akagi, "Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system", *IEEE Trans. on Power Electron.*, Vol. 22, No.1, pp. 1046-1053, May 2007.
- [17] B.N. Singh, P. Rastgoufard, B. Singh, A. Chandra and K.Al. Haddad, "Design, simulation and implementation of

three pole/ four pole topologies for active filters”, *IEEE Electr. Power Appl.*, Vol. 151, No. 4, pp. 467-476, July 2004.



Bhim Singh (SM'99) was born in Rahamapur (UP), India, in 1956. He received the B.E (Electrical) degree from the University of Roorkee, Roorkee, India, in 1977 and the M.Tech and Ph.D. degree from the Indian Institute of Technology (IIT)

Delhi, New Delhi, India, in 1979 and 1983, respectively. In 1983, he joined the Department of Electrical Engineering, University of Roorkee, as a lecturer, and in 1988 became a Reader. In December 1990, he joined the Department of Electrical Engineering, IIT Delhi, as an Assistant Professor. He became an Associate Professor in 1994 and Professor in 1997. His area of interest includes power electronics, electrical machines and drives, active filters, FACTS, HVDC and power quality. Dr. Singh is a fellow of Indian National Academy of Engineering (INAE), the Institution of Engineers (India) (IE (I)), and the Institution of Electronics and Telecommunication Engineers (IETE), a life member of the Indian Society for Technical Education (ISTE), the System Society of India (SSI), and the National Institution of Quality and Reliability (NIQR) and Senior Member of Institute of Electrical and Electronics Engineers (IEEE).

Visiting Professor at the Royal Melbourne Institute of Technology, Melbourne, Australia, in 1982 and 1989. He was a National Science Foundation Fellow at Purdue University, West Lafayette, IN, in 1992. He was Principal of Visvesvarayya Regional Engineering College, Nagpur, India, during 1997–1998. Prof. Kothari has received several best paper awards and gold medals for his work.



P. Jayaprakash is on deputation for research in the Indian Institute of Technology, Delhi, from the Department of Electrical and Electronics Eng., Govt. College of Eng. Kannur, Kerala. He received his B.Tech (University of Calicut, Kerala) and M.Tech (IIT Delhi) in 1996 and 2003 respectively. His fields of interest

are power quality, power electronics, power systems, etc.



D. P. Kothari (SM'03) received his B.E. (Electrical), M.E. (Power Systems), and Doctoral degree in electrical engineering from BITS, Pilani, India. Presently, he is Vice Chancellor of Vellore Institute of Technology, Vellore, Tamil Nadu, India. He was a

Professor and a Centre for Energy Studies and Director I/C at Indian Institute of Technology, New Delhi. His activities include optimal hydro-thermal scheduling, unit commitment, maintenance scheduling, energy conservation and power quality. He has guided 16 Ph.D scholars and has contributed extensively in these areas as evidenced by the 335 research papers authored by him. He has also authored 15 books on power systems. He was a